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EXAMINER	
LE, DUNG ANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,324	CHEN ET AL.	
	Examiner	Art Unit	
	DUNG A LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-49 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 June 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/3/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DLe

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 6/24/03 is acceptable.

Election/Restriction

Application's election **without traverse** of Group II (Claims 1- 32) drawn to process of making a semiconductor device is acknowledged for prosecution in the subject application . Applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims.

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on **11/03/2003** and made of record . The references cited on the PTOL 1449 form have been considered.

Specification

The specification is objected to for the following reason:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed (see MPEP § 606.01).

A new abstract is required that is clearly indicative the invention to which the claims are directed. Note that, the claims are directed to a method of making a semiconductor device instead of to a semiconductor device.

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 112

Claim 22 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 22, the language of " the layers " is insufficient antecedent basis for this limitation in the claim. Note that, claim 21 provides the antecedent basic for this term.

The remaining claims (23-25) are dependent from the above rejected claims and therefore also considered indefinite.

Set of claims 1-5

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 3 and 5 are rejected under 35 USC 102 (b) as being anticipated by Nitta et al. (6784054 B2).

Nitta et al. a method of fabricating a memory cell, comprising:

forming a silicide layer 121 on a word line of the memory cell concurrently with forming a silicide layer 121 on a contact to a source/drain region111s/113d of the memory cell (fig. 8A-8B).

Regarding claim 2, wherein forming a silicide layer 121comprises forming a self-aligned silicide layer (fig. 8B).

Regarding claim 3, wherein forming a silicide layer further comprises forming alayer of sifcide selected from the group consisting of chromium silicide, cobalt silicide, hafnium silicide, molybdenum silicide, niobium silicide. tantalum silicide, titanium silicide, tungsten silicide (col 2, line 29) , vanadium silicide and zirconium silicide.

Regarding claim 5, further comprising forming the silicide layer 121 on the word line of the memory cell concurrently with forming a silicide layer 121 on a contact to each of a drain region of the memory ecll and a source region of the memory cell (fig. 8B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Nitta et al. in view of the following remark.

Nitta et al. discloses the claimed invention as applied to claim 1 except for wherein forming a silicide layer further comprises forming alayer of silicide selected from the group consisting of titanium silicide and cobalt silicide.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a silicide layer further comprises forming alayer of silicide selected from the group consisting of titanium silicide and cobalt silicide, because the

identified materials are commonly used to prevent undesirable reactions in the contact region and improved the conductivity of the device, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Set of claims 6-10

Claims 6- 9 are rejected under 35 USC 102 (b) as being anticipated by Nitta et al. (6784054 B2).

Nitta et al. teaches method of fabricating an array of floating-gate memory cells, comprising:

forming a layer 121 of silicide on one or more word lines of the array, each word line extending to a plurality of columns of the array: while forming the layer of silicide on the one or more word lines, forming a layer of silicide on one or more contacts 115b to drain regions 113d of the memory cells; and while forming the layer of silicide 121 on the one or more word lines, forming a layer of silicide on one or more interconnects 115a to source regions 111s of the memory cells, wherein each interconnect contacts source regions of memory cells of one or more columns of the array (fig. 8A-8B).

Regarding claim 7, wherein each interconnect contacts source regions 111s to memory cells of the same number of columns 115aas an associated word line.

Regarding claim 8, wherein forming the layer of silicide on the one or more wordlines of the array, forming the layer of silicide on the one or more contacts 115a/115b to drain regions113d of the memory cells and forming the layer of silicide on the one or more interconnects to source regions of the memory cells further comprises: forming a layer of refractory metal on the word lines, contacts to drain regions, interconnects to source regions and interposing structures; reacting the refractory metal with free silicon in the word lines, contacts to drain regions and interconnects to source regions; and removing unreacted refractory metal from the interposing structures (fig. 8b).

Regarding claim 9, wherein forming the layer of refractory metal further comprises forming a layer of refractory metal selected from the group consisting of chromium, cobalt, hafnium, molybdenum, niobium, tantalum, titanium, tungsten, vanadium and zirconium.(col 2, line 29).

Claim 10 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Nitta et al. in view of the following remark.

Nitta et al. discloses the claimed invention as applied to claim 6, except for wherein forming a silicide layer further comprises forming alayer of silicide selected from the group consisting of titanium silicide and cobalt silicide.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a silicide layer further comprises forming alayer of silicide selected from the group consisting of titanium silicide and cobalt silicide, because the identified materials are commonly used to prevent undesirable reactions in the contact region and improved the conductivity of the device, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Set of claims 11- 20.

Claims 11- 20 are rejected under 35 USC 102 (b) as being anticipated by Nitta et al. (6784054 B2).

Natted et al. teaches a method of forming a floating-gate memory cell, comprising:

forming a word line stack (fig. 3), comprising: forming a tunnel dielectric layer 101 overlying a semiconductor substrate 100;

forming a floating-gate layer 102 overlying the tunnel dielectric layer;

forming an intergate dielectric layer 103 overlying the floating-gate layer;

forming a polysilicon control gate layer 105 overlying the intergate dielectric layer; and

forming a sacrificial cap layer 107h overlying the polysilicon control gate layer;

forming dielectric spacers (fig. 5B) on sidewalls 114a of the word line stack;

forming a drain region 113d in the substrate on a first side of the word line stack;

forming a source region 111s in the substrate on a second side of the word line stack;

forming a first polysilicon contact to the source region 115;

removing the cap layer 107h, thereby exposing the polysilicon control gate layer 105c ; and forming silicide layers concurrently on the polysilicon control gate layer and the first polysilicon contact (fig. 8A-8B).

Regarding claim 12, wherein the drain and source regions are formed after forming the word line stack (fig. 4A).

Regarding claim 13, forming the sacrificial cap107 layer further comprises forming the sacrificial cap layer of a first dielectric material; and forming the dielectric spacers 114 further comprises forming the dielectric spacers of a second dielectric material different from the first dielectric material (col 8, line 22).

Regarding claim 14, wherein forming the first polysilicon contact further comprises: forming an insulator layer 112 overlying the word line stack, the drain region and the source region; removing a first portion of the insulator layer to expose the cap layer; removing a second portion of the insulator layer to expose the source region; forming a polysilicon layer in contact with the source region (fig. 4a- 4b).

Regarding claim 15, wherein removing the first portion of the insulator further comprises planarizing the insulator layer using the cap layer 107h as a stop layer (fig. 6c).

Regarding claim 16, wherein removing the second portion of the insulator layerfurther comprises forming a mask overlying the planarized insulator layer to expose portions of the insulator layer to be removed and etching the exposed portions of the insulator layer to expose the source region (figs 4A- 4B).

Regarding claim 17, further comprising:

forming a second polysilicon contact to the drain region; and

forming silicide layers concurrently on the polysilicon control gate layer, the first polysilicon contact and the second polysilicon contact (fig. 8B).

Regarding claim 18, wherein forming the first polysilicon contact and forming the second polysilicon, contact further comprises:

forming an insulator layer overlying the word line stack, the drain region and the source region;

removing a first portion of the insulator layer to expose the cap layer;

removing a second portion of the insulator layer as a contact hole to expose the drain region;

removing a third portion of the insulator layer as a trench to expose the source region;

forming a polysilicon layer filling the contact hole and the trench. (figs 4A-4B).

Regarding claim 19, wherein forming the polysilicon layer 115 further comprises forming a blanket layer of polysilicon and planarizing the blanket layer of polysilicon using the cap layer as a stop layer. (fig. 6C)

Regarding claim 20, forming the sacrificial cap layer further comprises forming the sacrificial cap layer of a first dielectric material; and

forming the dielectric spacers further comprises forming the dielectric spacers of asecond dielectric material different from the first dielectric material. (figs 5A- 5B).

Set of claims 21- 32

Claims 21, 26- 30are rejected under 35 USC 102 (b) as being anticipated by Nitta et al. (6784054 B2).

Nitta et al. disclose a method of forming an array of floating-gate memory cells, comprising:

forming a first dielectric layer 101 on a silicon substrate 100;

forming a first polysilicon layer 102 on the first dielectric layer;

forming a second dielectric layer 105 on the first polysilicon layer 102; forming a second polysilicon layer on the second dielectric layer 103; forming a third dielectric layer 107 on the second polysilicon layer;

patterning the first dielectric layer, the first polysilicon layer, the second dielectric layer, the second polysilicon layer and the third dielectric layer to define word line stacks; (fig. 3A-3B).

forming source and drain regions between adjacent word line stacks (Fig. 4A-4B); forming dielectric spacers on sidewalls of the word line stacks;

forming an insulator layer 112 between adjacent word line stacks;

removing a portion of the insulator layer to define contact holes exposing drain regions and trenches exposing source regions, wherein each contact hole exposes one drain region and wherein each trench exposes a plurality of source regions (Fig. 4A-4B);;

filling the contact holes and trenches with a third polysilieon layer 115; removing the third dielectric layer, thereby exposing the second polysilicon layer 105 (fig. 7c);

forming a silicide layer 121 on the second polysilicon layer; and forming a silicide layer 121 on the third polysilicon layer (Fig. 8B).

Regarding claims 22- 25, see 112 rejection above.

Regarding claim 26, wherein forming the silicide layer 121 on the second polysilicon layer occurs concurrently with forming the silicide layer on the third polysilicon layer.

Regarding claim 27, wherein forming the silicide layer 121 on the second polysilicon layer and forming the silicide layer on the third polysilicon layer further comprise forming a self-aligned silicide layer on the second and third polysilicon layers (fig. 8B).

Regarding claim 28, wherein forming the self-aligned silicide layer on the second arid third polysilicon layers further comprises forming a self-aligned silicide layerusing a refractory metal selected from the group consisting of chromium, cobalt, hafnium, molybdenum, niobium, tantalum, titanium, tungsten (col 2, line29) , vanadium and zirconium.

Regarding claim 29, wherein forming the self-aligned silicide layer on the second and third polysilicon layers further comprises forming a self-aligned silicide layer using a refractory metal selected from the group consisting of cobalt and titanium.

Regarding claim 30, wherein removing a portion-of the insulator layer 112 to define trenches exposing source regions 111s further comprises exposing source regions along an entire length of a word line stack (fig. 4A) .

Claims 31-32 arerejected under 35 U.S.C. 103 (a) as being unpatentable over Nitta et al. in view of the following remark.

Nitta et al. discloses the claimed invention as applied to claim 21, except for steps forming a bit line coupled to drain regions of a column of memory cells, wherein the bit line is individually coupled to each drain region of the column of memory cells; forming at least one contact to a word line stack of a row of memory cells; and forming at least one contact to source regions of the row of memory cells (as cited in claim 31), forming only one contact to the word line stack of the row of memory cells; and forming only one contact to the source regions of the row of memory cells (as cited in claims 32).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to connect the above-device to surrounding region by performing the identified steps, since it has been held to be within the general skill of a worker in the art to select a connecting on the basis of its suitability for the intended use.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Primary Examiner
Art Unit 2818